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(54) Active matrix substrate

Substrat mit aktiver Matrix

Substrat à matrice active

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Description

[0001] The present invention relates to an active-matrix liquid crystal display device, and particularly to a planarizing technique for an active-matrix substrate on which pixel electrodes and thin film transistors (TFT) for switching are integrally formed.

Description of the Related Art

[0002] A general construction of a prior art active-matrix liquid crystal display device will be briefly described with reference to Fig. 3. Each thin film transistor 3802 is integrally formed on the surface of a lower substrate 3810. A metal bus line pattern 3804 is electrically connected to a source region S of the thin film transistor 3802 through a first layer insulating film 3803. A pixel electrode 3806 is electrically connected to a drain region D of the thin film transistor 3802 through the first layer insulating film 3803 and a second layer insulating film 3805. The surface of the second layer insulating film 3805 is covered with an alignment film 3807. (Hereinafter, the lower substrate 3801 on which each thin film transistor 3802 and each pixel electrode 3806 are thus integrally formed is referred to as "active-matrix substrate" or "TFT substrate"). An upper substrate 3808 is disposed so as to face to the active-matrix substrate 3801 with a specified interval. A facing electrode 3809 and an alignment film 3810 are formed on the inner surface of the upper substrate 3808. (Hereinafter, such an upper facing substrate 3808 is referred to as "facing substrate"). A liquid crystal 3811 controlled in its alignment by the alignment films 3807 and 3810 is inserted in the interval between both the substrates 3801 and 3808. In the active-matrix liquid crystal display device having the above construction, when an image signal is supplied through the metal bus line pattern 3804 while a selection signal is applied to a gate electrode G of the thin film transistor 3802, a specified signal load is written on the pixel electrode 3806. The molecular alignment of the liquid crystal 3811 is changed depending on the voltage generated between the pixel electrode 3806 and the facing electrode 3810, to perform the desired image display.

[0003] Further, a general construction of a prior art active-matrix liquid crystal display device will be briefly described with reference to Fig. 6. The active-matrix liquid crystal display device has a cell structure including a pair of substrates 4101 and 4102 disposed so as to face to each other with a specified interval, and a liquid crystal layer 4103 held in the interval. One substrate 4101 is formed with pixel electrodes 4104 arranged in a matrix in the vertical and lateral directions, and switching devices connected to the individual pixel electrodes 4104. In this example, the switching devices comprise thin film transistors (TFT). In each TFT, a drain electrode is connected to the corresponding pixel electrode 4104; a source electrode is connected to a signal line 4105; and a gate electrode is connected to agate line 4106. (Hereinafter, the substrate 4101 having such a construction is referred to as "TFT substrate"). The other substrate 4102 includes a facing electrode 4107 for applying a vertical electric field to the liquid crystal layer 4103. In addition, the other substrate 4102 includes a color filter layer 4108. The color filter layer 4108 has segments divided into the primary colors, that is, red, green and blue. The segments are each matched with the pixel electrodes 4104. A pair of polarization plates 4109 and 4110 are stuck on both the surfaces of the cell structure.

[0004] The TFTs are selected in a line-sequential manner for each line through the gate line 4106, and an image signal is supplied to the TFTs through the signal line 4105, to perform the desired full color image display. The liquid crystal layer 4103 is, for example, in the twisted nematic alignment, so that the molecular alignment of the liquid crystal layer 4103 is changed in response to the vertical electric field applied between the facing electrode 4107 and each pixel electrode 4104. The change in the molecular alignment is taken off as the change in a transmitted light amount by a pair of the polarization plates 4109 and 4110, to thus perform the image display.

[0005] For the twisted nematic alignment of the liquid crystal layer 4103, the inner surfaces of a pair of the upper and lower substrates 4101 and 4102 must be subjected to an alignment treatment. The alignment treatment includes, for example, forming a specified alignment film and then rubbing the alignment film. Fig. 7 is a typical view showing the rubbing treatment. In this example, as shown in the figure, the inner surface of the lower TFT substrate 4101 is rubbed in the direction R, that is, bottom-to-top, while the inner surface of the facing substrate 4102 is rubbed in the direction R, that is, right-to-left. When a liquid crystal layer is sealingly inserted between a pair of the substrates 4101 and 4102 thus obtained, the liquid crystal molecules of the liquid crystal layer are twisted by 90°.

[0006] In the prior art structure shown in Fig. 3, wherein the thin film transistors 3802 and the metal bus line patterns 3804 are integrally formed on the active-matrix substrate 3801, the surface of the substrate 3801 is quite uneven, that is, has numerous irregularities and stepped portions. This makes it difficult to perform the alignment control for the liquid crystal 3811 and to obtain the uniform image display. The alignment of the liquid crystal is disturbed particularly in the stepped portions, which tends to cause the reverse tilt domain where the pretilt angle is reversed, thereby deteriorating the display quality. For shielding the region disturbed in the alignment, there has been known a technique of forming a black mask on the facing substrate side. The black mask is usually provided so as to be overlapped on the end portion of the pixel electrode liable to be disturbed in the alignment, thus sacrificing the effective display region. As a result, in aiming at enhancing the density of the pixel electrodes arranged in a matrix by reduction of

the arrangement pitch thereof, the aperture ratio is lowered because the width of the black mask pattern cannot be reduced. Further, along with the reduction of the pixel pitch and the miniaturization of the chip size, the prior art structure has the following various disadvantages in terms of the manufacturing processes. For example, the thickness of the alignment film becomes uneven because of the large irregularities on the surface of the active-matrix substrate. This makes also difficult the uniform rubbing treatment for the alignment film. Further, when the active-matrix substrate is adhesively bonded with the facing substrate, there occurs a faulty in adhesiveness because of the irregularities. Additionally, in the prior art structure, the direction of the electric field applied to the liquid crystal is made uneven by the effect of the irregularities on the surface of the active-matrix substrate, which obstructs the control to obtain the uniform transmissivity. The liquid crystal is changed in its alignment depending on the electric field applied between each pixel electrode and the facing electrode, to be thus ON-OFF controlled. However, when the metal bus line and the gate line are raised around the pixel electrodes, the liquid crystal is affected by the lateral electric field. This disturbs the normal action by the synergistic effect with the disorder of the pretilt angle.

[0007] Along with the strong demands toward the fineness and accuracy in the active-matrix liquid crystal display device, the pixel pitch has been made small. To meet the above demands, it is required to enlarge the area of the pixel electrode as much as possible for ensuring the desired aperture ratio. Consequently, the interval between the adjacent pixel electrodes becomes smaller. In the extreme case, the interval between the adjacent pixel electrodes is made smaller than the interval between each pixel electrode and the facing electrode, so that the liquid crystal is occasionally affected by the subsidiary lateral electric field generated between the adjacent pixel electrodes larger than the normal vertical electric field applied between each pixel electrode and. the facing electrode. In fact, the prior art structure has the following disadvantages: namely, by the effect of the lateral electric field, the reverse tilt domain is generated in the liquid crystal layer; and the light fallout is generated because the liquid crystal molecules are not correctly raised, resulting in the poor image quality.

[0008] Fig. 4 is a sectional view showing the construction of a prior art active-matrix liquid crystal display device. In this prior art structure, a pixel electrode 3906 is provided on a recessed portion surrounded by bus lines 3904 or the like arranged in a matrix. Accordingly, liquid crystal pixels are separated from each other. However, as the arrangement pitch is made fine along with the demands toward the high accuracy and fineness of the liquid crystal display device, the alignment defect of the liquid crystal 3903 is generated by the irregularities on the surface of the substrate. For example, when the substrate 3901 is rubbed in the direction of the arrow, liquid crystal molecules 3908 in the upper area of the pixel electrode 3906 have a specified pretilt angle, that is, are in the normal tilt state. In the areas near the tilt surfaces 3909 being the shady sides in the rubbing direction, the liquid crystal molecules 3908 are raised in the direction opposed to the normal tilt state, and are thus in the reverse tilt state. Consequently, the disclination is generated at the boundary between both the states, which deteriorates the display quality.

[0009] Fig. 5 is a typical view of the prior art structure shown in Fig. 4. As described above, since each pixel electrode 3906 is formed on a recessed portion surrounded by bus lines 3904, adjacent liquid crystal pixels are structurally separated from each other. However, it is difficult to apply the uniform rubbing treatment for the surface having the significant irregularities. In particular, as the arrangement pitch of the pixel electrodes is made fine along with the demands toward the high accuracy and high fineness of the display device, the irregularities on the surface of the substrate is made relatively significant, tending to often cause the alignment defect.

[0010] various means have been proposed to prevent the generation of the reverse tilt state. For example, Japanese Patent Laid-open No. HEI 4-305625 discloses a technique of forming grooves on a substrate for embedding thin film transistors and bus lines therein, thereby reducing the irregularities on the surface. Further, Japanese Patent Laid-open No. HEI 4-320212 discloses a technique of forming grooves in a layer insulating film for preventing the enlargement of the reverse tilt state. These techniques, however, fail to perfectly prevent the reverse tilt state.

[0011] Fig. 8 is a typical plan view of a TFT substrate. As shown in the figure, individual pixel electrodes are arranged in a matrix. They are repeatedly arranged in order of red, blue and green along the line direction. On the other hand, they are not linearly arranged in a row direction, and are shifted to each other by a half pitch in the lateral direction. As a result, the adjacent red, green and blue pixels are arranged in a triangular shape, that is, are in the delta arrangement, thus apparently improving the resolution. Each pixel electrode 4301 has an asymmetric shape in the right and left, and is provided with a portion to be matched with a contact hole C of a TFT (not shown).

[0012] In the liquid crystal display device, there is generally performed the A.C reverse drive, for example, the so-called 1H drive wherein the polarity of a signal. voltage applied to pixel electrodes is reversed for each line. When the laster display is made by 1H drive, for example, (the center level of the signal voltage + the maximum signal voltage) are applied to pixel electrodes in the first line; and (the center level of the signal voltage - the maximum signal voltage) are applied to pixel electrodes in the second line. Accordingly, a large potential difference ΔV is generated between the vertically adjacent pixel electrodes 4301, which is twice as much as the maximum signal voltage. As the arrangement pitch between the pixel electrodes is made fine along with the

demands toward the high accuracy and high fineness of the active-matrix liquid crystal display device, a lateral electric field intensity generated due to the above potential difference ΔV cannot be neglected as compared with the vertical electric field intensity generated between the facing electric electrode and the pixel electrodes. In addition, the lateral electric field is generated in the plane direction of the figure, and the vertical electric field is generated in the direction vertical to the figure (in the thickness direction of the liquid crystal).

[0013] In the delta arrangement shown in Fig. 8, each pixel electrode 4301 has an asymmetric shape in the right and the left. Accordingly, between the pixel electrode in the first and second lines, the lateral electric field intensity is maximized at a region A, and minimized at a region B. Because of the unbalance of the lateral electric field intensities between the regions A and B, the liquid crystal molecules positioned on the lower portion of the pixel electrode in the first line are applied with a force F directed from the right to the left. On the other hand, as for the lateral electric field generated between the pixel electrodes generated in the second and the third lines, the above strong region A becomes weak, and the above weak region B becomes strong. Accordingly, the liquid crystal molecules positioned on the lower portion of the pixel electrodes in the second line is applied with a force F directed from the left to the right.

[0014] On the other hand, as described above with reference to Fig. 7, when the TFT substrate is rubbed in the direction R from the bottom to the top and the facing substrate is rubbed in the direction R from the right to the left, the rotational direction T of the liquid crystal molecules M becomes clockwise as seen from the facing substrate side in Fig. 8. In the first line, the liquid crystal molecules M is applied with the force F in the direction reversed to the rotational direction T, so that they tend to be rotated in the reversed direction against the dominating force of the vertical electric field, thus enlarging the so-called reverse tilt domain. On the other hand, in the second line, the liquid crystal molecules M is applied with a force F in the direction similar to the rotational direction T, so that they are raised rapidly in the normal direction, thus reducing the reverse tilt domain. As is apparent from the above description, for the pixel electrode having an asymmetric shape in the right and the left, by actually performing the 1H drive, the magnitudes of the reverse tilt domains becomes different.

[0015] Fig. 9 is a sectional view taken along the line Y-Y of the active-matrix liquid crystal display device of Fig. 8. From the left to the right in the figure, there are shown part of a pixel electrode in the first line, a pixel electrode in the second line, and part of a pixel electrode in the third line. As described above, a large reverse tilt domain region LRTD is generated between pixel electrodes in the first and second lines, and only a small reverse tilt domain region SRTD is generated between pixel electrodes in the second and the third lines. Since the reverse tilt domain regions reduce the display quality, they are generally shielded by black masks. As shown in the figure, a black mask 4411 is provided, for example, on the inner surface of a facing substrate 4402. The plane dimension of the black mask 4411 must be set to shield the large reverse tilt domain region LRTD. Accordingly, in the case that the reverse tilt domains are varied for each line due to the laterally asymmetric shape of each pixel electrode just 'as the prior art, the dimension of the black mask 4407 must be necessarily enlarged. This causes the disadvantage of sacrificing the aperture ratio of the active-matrix liquid crystal display device.

[0016] The JP-A-01 156 725 discloses a display device wherein the quality of an image is improved by arranging picture element electrodes on an insulating film which covers at least a part of an active element and a wiring. The wiring operates as a light shield layer and light transmitted through other parts is used effectively to obtain a bright picture with a high contrast ratio.

[0017] In the JP-A-59 172 627 a display panel is described wherein an insulating film is formed of an organic resin for covering and planarizing a layer consisting of pixel electrodes and thin film transistors. On the insulating film a light shading film is formed for intercepting light incident on regions where the thin film transistors are formed.

[0018] The JP-A-62 254 122 comprises a thin film transistor integrated color liquid crystal display device in which the color filters are provided on the lower substrate so as to utilize the difference in level which is produced due to the formation of thin film transistors on the lower substrate.

[0019] The JP-A-04 323 625 describes a liquid crystal device intends to prevent the generation of a reverse tilt domain and to improve the contrast of display images. This is achieved by setting the distance between a picture element electrode and a signal bus line on the rear side of the rubbing direction on the picture element electrode side larger than the gap between the picture element electrode and a counter electrode.

[0020] The same object is addressed in the JP-A-04 320 212. In the liquid crystal display device described therein a groove is formed between a picture element electrode and a bus line. The device as depicted therein also shows a light shield layer formed on the upper substrate above the transistor and the bus line.

[0021] It is an object of the present invention to provide an active-matrix substrate, in particular for use in an active-matrix liquid crystal device, which comprises a good contrast ratio even for greater viewing angles.

[0022] This object is achieved with an active-matrix substrate and an active-matrix liquid crystal device according to the features of the appended independent claims 1 to 4.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023]

Fig. 1 is a typical view showing a shading structure of an active-matrix substrate of the present invention;
Fig. 2 is a sectional view showing one example of an active-matrix color liquid crystal display device of the present invention;
Fig. 3 is a sectional view showing a general example of a prior art active-matrix substrate;
Fig. 4 is a typical sectional view showing the construction of a prior art active-matrix liquid crystal display device;
Fig. 5 is a typical perspective view of a prior art active-matrix liquid crystal display device;
Fig. 6 is a perspective view of a general construction of a prior art active-matrix liquid crystal display device;
Fig. 7 is a typical view showing a rubbing treatment;
Fig. 8 is a typical plan view showing a shape and an arrangement of each pixel electrode of a prior art active-matrix liquid crystal display device; and
Fig. 9 is a view for explaining the problem of a prior art active-matrix liquid crystal display device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0024] Hereinafter, embodiments of the inventive device will be described in conjunction with the drawings.

[0025] Fig. 1 is a typical sectional view showing one example of a shading structure of an active-matrix substrate according to the present invention. As described above, the boundary portion between adjacent pixel electrodes can be at least partially shielded using a metal bus line pattern as a black mask. However, the portion of a TFT 1559 cannot adopt this shielding structure. In the structure shown in Fig. 1, for selectively shielding the TFT portion, a shading layer 1551 made from metal is used. As shown in the figure, the TFTs are integrally formed on the surface of a substrate 1552. A layer insulating film 1553 is formed for covering the TFT. A metal bus line pattern 1555 is electrically connected to a source region S of the TFT by way of a first contact hole 1554 through the layer insulating film 1553. The TFT 1559 is shielded by the shading layer 1551 formed by patterning in a specified shape. Further, a planarization film 1556 is formed on the TFT for embedding the irregularities on the surface of the TFT. A pixel electrode 1558 is electrically connected to a drain region D of the TFT by way of a second contact hole 1557 passing through the planarization film 1556, the shading layer 1551 and the layer insulating film 1553. In this example, by use of the shading layer 1551, the TFT can be substantially perfectly shielded. However, the shading layer 1551 is removed from the second contact hole 1557, the leakage of light is slightly generated in the second contact hole 1557.

[0026] Fig. 2 is a typical sectional view showing an embodiment wherein a planarization film of the present invention is used as a color filter in an active-matrix liquid crystal display device. As shown in the figure, this color liquid crystal display device includes an active-matrix substrate 1771 and a facing substrate 1772 which are disposed to face to each other with a specified interval, and a liquid crystal 1773 inserted in the interval between both the substrates. TFTs 1700 are integrally formed on the surface of an insulating substrate 1774. The TFTs 1700 includes first polysilicons 1775 formed by patterning in a dotted pattern, and gate electrodes 1777 formed by patterning through a gate insulating film 1776. The gate electrode 1777 is made from, for example a second polysilicon. The TFT 1700 is covered with a first layer insulating film 1778. A metal bus line pattern 1780 is electrically connected to a source region S of the TFT by way of a first contact hole 1779 provided on the first layer insulating film 1778. The metal bus line pattern 1780 is covered with a second layer insulating film 1781, on which a passivation film 1782 is formed by patterning. The passivation film 1782 is made from, for example p-SiN formed by a plasma CVD method. A shading film 1783 is formed on the passivation film 1782, to shield the TFT. A planarization film 1784 is deposited to embed the irregularities on the TFT and the metal bus line film 1780. The planarization film 1784 has a film thickness of at least 2.0μm enough to embed the irregularities of about 1μm to 2μm. A second contact hole 1785 is provided so as to pass through the planarization film 1784, the second layer insulating film 1781 and the first layer insulating film 1778. The interior and the periphery of the second contact hole 1785 are covered with the shading layer 1786. A pixel electrode 1787 is electrically connected to a drain region D of the TFT through the second contact hole 1785. This embodiment has a feature in that the portion of the planarization film 1784 matched with the pixel electrode 1787 is colored in a specified hue, to form a color filter. The selective coloring of the planarization layer 1784 can be. made by use of, for example a pigment diffusion method. Differently from the prior art, the color filter is provided integrally on the active-matrix substrate 1771 side, which eliminates the alignment margin between the pixel electrode and the color filter. In addition, the surface of the pixel electrode 1787 is covered with an alignment film 1788.

[0027] On the other hand, a facing electrode 1789 and an alignment film 1790 are formed on the inner surface of the facing electrode 1772 so as to overlapped to each other. The liquid crystal 1773 held by a pair of the upper and lower alignment films 1790 and 1788 is uniformly controlled in a desired alignment state.

Claims

1. An active-matrix substrate (1552) comprising:

   an upper region having a plurality of pixel electrodes (1558) arranged in a matrix;
   a lower region having a plurality of thin film transistors (1559) each of which is associated to a corresponding pixel electrode (1558); and
   a planarization layer (1556) arranged between the upper and lower regions to planarize a surface of the lower region, and
   a black mask formed at a boundary between adjacent pixel electrodes (1558),
   a layer insulating film (1553) covering the thin film transistors (1559),
   a metal bus line pattern (1555) electrically connected to a source region (S) of each thin film transistor (1559) by way of a first contact hole (1554) through the layer insulating film (1553),
   the black mask being comprised of a shading layer (1551) formed above each thin film transistor (1559) on the metal bus line pattern (1555) and the layer insulating film (1553),
   the planarization layer (1556) being formed on the shading layer (1551) and the layer insulating film (1553),
   the pixel electrode (1558) being electrically connected to a drain region (D) of the thin film transistor (1559) by way of a second hole (1557) passing through the planarization film (1556), the shading layer (1551) and the layer insulating film (1553).

2. An active-matrix liquid crystal display device, comprising:

   first and second substrates arranged in parallel to each other,
   the first substrate (1552) comprising an upper region which has a plurality of pixel electrodes (1558) arranged in a matrix, a lower region which has a plurality of thin film transistors (1559), each of which is associated to a corresponding pixel electrode (1559), and a planarization layer (1556) arranged between the upper and lower regions to planarize
   a surface of the lower region,
   a black mask formed at a boundary between adjacent pixel electrodes (1558); and
   a liquid crystal layer formed between the first and second substrates,

   said first substrate further comprising

   a layer insulating film (1553) covering the thin film transistors (1559),
   a metal bus line pattern (1555) electrically connected to a source region (S) of each thin film transistor (1559) by way of a first contact hole (1554) through the layer insulating film (1553),
   the black mask being comprised of a shading layer (1551) formed above each thin film transistor (1559) on the metal bus line pattern (1555) and the layer insulating film (1553),
   the planarization layer (1556) being formed on the shading layer (1551) and the layer insulating film (1553),
   the pixel electrode (1558) being electrically connected to a drain region (D) of the thin film transistor (1559) by way of a second hole (1557) passing through the planarization film (1556), the shading layer (1551) and the layer insulating film (1553).

3. An active-matrix substrate (1774) comprising:

   an upper region having a plurality of pixel electrodes (1787) arranged in a matrix;
   a lower region having a plurality of thin film transistors (1700) each of which is associated to a corresponding pixel electrode (1787); and
   a planarization layer (1784) arranged between the upper and lower regions to planarize a surface of the lower region, and
   a black mask formed at a boundary between adjacent pixel electrodes (1787),
   a first layer insulating film (1778) covering the thin film transistors (1700),
   a metal bus line pattern (1780) electrically connected to a source region (S) of each thin film transistor (1700) by way of a first contact hole (1779) through the first layer insulating film (1778),
   a second layer insulating film (1781) covering the metal bus line pattern (1780) and the first layer insulating film (1778),
   a passivation film (1782) formed on the second layer insulating film (1781),
   the black mask comprising a shading film (1783) formed on the passivation film above a portion of the thin film transistor (1700),
   the planarization layer (1784) being formed on the shading film (1783) and the second layer insulating film (1781),
   the pixel electrode (1787) being electrically connected to a drain region (D) of the thin film transistor (1700) by way of a second hole (1785) passing through the planarization layer (1784) and the second layer insulating film (1781),
   the black mask further comprising a shading layer (1786) covering the interior and the periphery of the second contact hole.

4. An active-matrix liquid crystal display device, com-

prising:

first and second substrates arranged in parallel to each other,
the first substrate (1774) comprising an upper region which has a plurality of pixel electrodes (1787) arranged in a matrix, a lower region which has a plurality of thin film transistors (1700), each of which is associated to a corresponding pixel electrode (1787), and a planarization layer (1784) arranged between the upper and lower regions to planarize a surface of the lower region,
a black mask formed at a boundary between adjacent pixel electrodes (1787); and
a liquid crystal layer (1773) formed between the first and second substrates,

said first substrate further comprising

a first layer insulating film (1778) covering the thin film transistors (1700),
a metal bus line pattern (1780) electrically connected to a source region (S) of each thin film transistor (1700) by way of a first contact hole (1779) through the first layer insulating film (1778),
a second layer insulating film (1781) covering the metal bus line pattern (1780) and the first layer insulating film (1778),
a passivation film (1782) formed on the second layer insulating film (1781),
the black mask comprising a shading film (1783) formed on the passivation film above a portion of the thin film transistor (1700),
the planarization layer (1784) being formed on the shading film (1783) and the second layer insulating film (1781),
the pixel electrode (1787) being electrically connected to a drain region (D) of the thin film transistor (1700) by way of a second hole (1785) passing through the planarization layer (1784) and the second layer insulating film (1781),
the black mask further comprising a shading layer (1786) covering the interior and the periphery of the second contact hole.

Patentansprüche

1. Aktivmatrixsubstrat (1552) mit:

- einem oberen Bereich mit einer Vielzahl von in einer Matrix angeordneten Pixelelektroden (1558);
- einem unteren Bereich mit einer Vielzahl von Dünnschichttransistoren (1559), von denen jeder einer entsprechenden Pixelelektrode (1558) zugeordnet ist; und
- einer Einebnungsschicht (1556) zwischen dem oberen und dem unteren Bereich, um die Oberfläche des unteren Bereichs einzuebnen; und
- einer Schwarzmaske, die an der Grenze zwischen benachbarten Pixelelektroden (1558) ausgebildet ist;
- einem Schichtisolierfilm (1553), der die Dünnschichttransistoren (1559) bedeckt;
- einem Busleitungsmuster (1555) aus Metall, das über ein erstes Kontaktloch (1554) durch den Schichtisolierfilm (1553) mit dem Sourcebereich (S) jedes Dünnschichttransistors (1559) verbunden ist;
- wobei die Schwarzmaske aus einer über jedem Dünnschichttransistor (1559) auf dem Busleitungsmuster (1555) aus Metall und dem Schichtisolierfilm (1553) hergestellten Abschirmungsschicht (1551) besteht, wobei die Einebnungsschicht (1556) auf der Abschirmungsschicht (1551) und dem Schichtisolierfilm (1553) ausgebildet ist;
- wobei die Pixelelektrode (1558) über ein zweites Loch (1557), das durch den Einebnungsfilm (1556), die Abschirmungsschicht (1551) und den Schichtisolierfilm (1553) hindurch geht, elektrisch mit dem Drain (D) des Dünnschichttransistors (1559) verbunden ist.

2. Flüssigkristall-Anzeigevorrichtung mit aktiver Matrix mit:

- einem ersten und einem zweiten Substrat, die parallel zueinander angeordnet sind;
- wobei das erste Substrat (1552) über einen oberen Bereich mit einer Vielzahl von in einer Matrix angeordneten Pixelelektroden (1558), einen unteren Bereich mit einer Vielzahl von Dünnschichttransistoren (1559), von denen jeder einer entsprechenden Pixelelektrode (1559) zugeordnet ist, und eine zwischen dem oberen und unteren Bereich zum Einebnen der Oberfläche des unteren Bereichs angeordnete Einebnungsschicht (1556) verfügt;
- einer Schwarzmaske, die an der Grenze zwischen benachbarten Pixelelektroden (1558) ausgebildet ist; und
- einer zwischen dem ersten und zweiten Substrat ausgebildeten Flüssigkristallschicht;

wobei das erste Substrat ferner mit Folgendem versehen ist:

- einem Schichtisolierfilm (1553), der die Dünnschichttransistoren (1559) bedeckt;
- einem Busleitungsmuster (1555) aus Metall, das über ein erstes Kontaktloch (1554) durch

den Schichtisolierfilm (1553) mit dem Sourcebereich (S) jedes Dünnschichttransistors (1559) verbunden ist;

- wobei die Schwarzmaske aus einer über jedem Dünnschichttransistor (1559) auf dem Busleitungsmuster (1555) aus Metall und dem Schichtisolierfilm (1553) hergestellten Abschirmungsschicht (1551) besteht, wobei die Einebnungsschicht (1556) auf der Abschirmungsschicht (1551) und dem Schichtisolierfilm (1553) ausgebildet ist;
- wobei die Pixelelektrode (1558) über ein zweites Loch (1557), das durch den Einebnungsfilm (1556), die Abschirmungsschicht (1551) und den Schichtisolierfilm (1553) hindurch geht, elektrisch mit dem Drain (D) des Dünnschichttransistors (1559) verbunden ist.

3. Aktivmatrixsubstrat (1774) mit:

- einem oberen Bereich mit einer Vielzahl von in einer Matrix angeordneten Pixelelektroden (1787);
- einem unteren Bereich mit einer Vielzahl von Dünnschichttransistoren (1700), von denen jeder einer entsprechenden Pixelelektrode (1787) zugeordnet ist; und
- einer Einebnungsschicht (1784), die zwischen dem oberen und dem unteren Bereich angeordnet ist, um die Oberfläche des unteren Bereichs einzuebnen; und
- einer Schwarzmaske, die an der Grenze zwischen benachbarten Pixelelektroden (1787) ausgebildet ist;
- einem ersten Schichtisolierfilm (1778), der die Dünnschichttransistoren (1700) bedeckt;
- einem Busleitungsmuster (1780) aus Metall, das über ein erstes Kontaktloch (1779) durch den ersten Schichtisolierfilm (1778) elektrisch mit dem Sourcebereich (S) jedes Dünnschichttransistors (1700) verbunden ist;
- einem zweiten Schichtisolierfilm (1781), der das Busleitungsmuster (1780) aus Metall und den ersten Schichtisolierfilm (1778) bedeckt;
- einem Passivierungsfilm (1782), der auf dem zweiten Schichtisolierfilm (1781) ausgebildet ist;
- wobei die Schwarzmaske über einen Abschirmungsfilm (1783) verfügt, der auf dem Passivierungsfilm über einem Teil des Dünnschichttransistors (1700) ausgebildet ist;
- wobei die Einebnungsschicht (1784) auf dem Abschirmungsfilm (1783) und dem zweiten Schichtisolierfilm (1781) ausgebildet ist;
- wobei die Pixelelektrode (1787) über ein zweites Kontaktloch (1785), das durch die Einebnungsschicht (1784) und den zweiten Schichtisolierfilm (1781) hindurch verläuft, elektrisch mit dem Drainbereich (D) des Dünnschichttransistors (1700) verbunden ist;
- wobei die Schwarzmaske ferner über eine Abschirmungsschicht (1786) verfügt, die das Innere und den Umfang des zweiten Kontaktlochs bedeckt.

4. Flüssigkristall-Anzeigevorrichtung mit aktiver Matrix mit:

- einem ersten und einem zweiten Substrat, die parallel zueinander angeordnet sind;
- wobei das erste Substrat (1552) über einen oberen Bereich mit einer Vielzahl von in einer Matrix angeordneten Pixelelektroden (1558), einen unteren Bereich mit einer Vielzahl von Dünnschichttransistoren (1559), von denen jeder einer entsprechenden Pixelelektrode (1559) zugeordnet ist, und eine zwischen dem oberen und unteren Bereich zum Einebnen der Oberfläche des unteren Bereichs angeordnete Einebnungsschicht (1556) verfügt;
- einer Schwarzmaske, die an der Grenze zwischen benachbarten Pixelelektroden (1558) ausgebildet ist; und
- einer zwischen dem ersten und zweiten Substrat ausgebildeten Flüssigkristallschicht;

wobei das erste Substrat ferner mit Folgendem versehen ist:

- einem ersten Schichtisolierfilm (1778), der die Dünnschichttransistoren (1700) bedeckt;
- einem Busleitungsmuster (1780) aus Metall, das über ein erstes Kontaktloch (1779) durch den ersten Schichtisolierfilm (1778) elektrisch mit dem Sourcebereich (S) jedes Dünnschichttransistors (1700) verbunden ist;
- einem zweiten Schichtisolierfilm (1781), der das Busleitungsmuster (1780) aus Metall und den ersten Schichtisolierfilm (1778) bedeckt;
- einem Passivierungsfilm (1782), der auf dem zweiten Schichtisolierfilm (1781) ausgebildet ist;
- wobei die Schwarzmaske über einen Abschirmungsfilm (1783) verfügt, der auf dem Passivierungsfilm über einem Teil des Dünnschichttransistors (1700) ausgebildet ist;
- wobei die Einebnungsschicht (1784) auf dem Abschirmungsfilm (1783) und dem zweiten Schichtisolierfilm (1781) ausgebildet ist;
- wobei die Pixelelektrode (1787) über ein zweites Kontaktloch (1785), das durch die Einebnungsschicht (1784) und den zweiten Schichtisolierfilm (1781) hindurch verläuft, elektrisch mit dem Drainbereich (D) des Dünnschichttransistors (1700) verbunden ist;
- wobei die Schwarzmaske ferner über eine Ab-

schirmungsschicht (1786) verfügt, die das Innere und den Umfang des zweiten Kontaktlochs bedeckt.

Revendications

1. Substrat (1552) à matrice active comprenant :

   une région supérieure possédant plusieurs électrodes d'élément d'image (1558) disposées suivant une matrice,
   une région inférieure ayant plusieurs transistors à couches minces (1559) associés chacun à une électrode correspondante d'élément d'image (1558),
   une couche (1556) de planarisation placée entre les région supérieure et inférieure afin que la surface de la région inférieure soit planaire,
   un masque noir formé à une limite entre des électrodes adjacentes d'éléments d'image (1558),
   un film isolant de couche (1553) recouvrant les transistors à couches minces (1559),
   un motif (1555) de lignes métalliques de bus connectées électriquement à une région de source (S) de chaque transistor à couches minces (1559) par un premier trou de contact (1554) formé dans le film isolant de couche (1553),
   le masque noir étant formé d'une couche d'ombrage (1551) formée au-dessus de chaque transistor à couches minces (1559) sur le motif (1555) de lignes métalliques de bus et le film isolant de couche (1553),
   la couche de planarisation (1556) étant formée sur la couche d'ombrage (1551) et le film isolant de couche (1553), et
   l'électrode d'élément d'image (1558) étant connectée électriquement à une région de drain (D) du transistor à couches minces (1559) par un second trou (1557) passant à travers le film de planarisation (1556), la couche d'ombrage (1551) et le film isolant de couche (1553).

2. Dispositif d'affichage à cristaux liquides à matrice active, comprenant :

   des premier et second substrats placés parallèlement l'un à l'autre,
   le premier substrat (1552) comprenant une région supérieure qui possède plusieurs électrodes d'éléments d'image (1558) disposés suivant une matrice, une région inférieure possédant plusieurs transistors à couches minces (1559) associés chacun à une électrode correspondante d'élément d'image (1559), et une couche de planarisation (1556) disposée entre les régions supérieure et inférieure afin qu'une surface de la région inférieure soit planaire,
   un masque noir formé à une limite entre des électrodes adjacentes d'élément d'image (1558),
   une couche de matière à cristaux liquides formée entre les premier et second substrats,
   le premier substrat comprenant en outre un film isolant de couche (1553) qui recouvre les transistors à couches minces (1559),
   un motif (1555) de lignes métalliques de bus, connectées électriquement à une région de source (S) de chaque transistor à couches minces (1559) par un premier trou de contact (1554) formé dans le film isolant de couche (1553),
   le masque noir étant formé d'une couche d'ombrage (1551) formée au dessus de chaque transistor à couches minces (1559) sur le motif (1555) de lignes métalliques de bus et le film isolant de couche (1553),
   la couche de planarisation (1556) étant formée sur la couche d'ombrage (1551) et le film isolant de couche (1553), et
   l'électrode d'élément d'image (1558) étant connectée électriquement à une région de drain (D) du transistor à couches minces (1559) par l'intermédiaire d'un second trou (1557) passant dans le film de planarisation (1556), la couche d'ombrage (1551) et le film isolant de couche (1553).

3. Substrat (1774) à matrice active, comprenant :

   une région supérieure ayant plusieurs éléments d'image (1787) disposés suivant une matrice,
   une région inférieure ayant plusieurs transistors à couches minces (1700) associés chacun à une électrode correspondante d'élément d'image (1787),
   une couche de planarisation (1784) disposée entre les régions supérieure et inférieure pour que la surface de la région inférieure soit planaire, et
   un masque noir formé à une limite entre des électrodes adjacentes d'élément d'image (1787),
   un premier film isolant de couche (1778) qui recouvre les transistors à couches minces (1700),
   un motif (1780) de lignes métalliques de bus connectées électriquement à une région de source (S) de chaque transistor à couches minces (1700) par un premier trou de contact (1779) formé dans le premier film isolant de couche (1778),
   un second film isolant de couche (1781) recou-

vrant le motif de lignes métalliques de bus (1780) et le premier film isolant de couche (1778),
un film de passivation (1782) formé sur le second film isolant de couche (1781),
un masque noir comprenant un film d'ombrage (1783) formé sur le film de passivation au dessus d'une partie du transistor à couches minces (1700),
la couche de planarisation (1784) étant formée sur le film d'ombrage (1783) et le second film isolant de couche (1781),
l'électrode d'élément d'image (1787) étant connectée électriquement à une région de drain (D) du transistor à couches minces (1700) par un second trou (1785) passant dans la couche de planarisation (1784) et le second film isolant de couche (1781),
le masque noir comprenant en outre une couche d'ombrage (1786) qui recouvre l'intérieur et la périphérie du second trou de contact.

4. Dispositif d'affichage à cristaux liquides à matrice active, comprenant :

des premier et second substrats placés parallèlement l'un à l'autre,
le premier substrat (1774) comprenant une région supérieure qui possède plusieurs électrodes d'éléments d'image (1787) disposés suivant une matrice, une région inférieure possédant plusieurs transistors à couches minces (1700) associés chacun à une électrode correspondante d'élément d'image (1787), et une couche de planarisation (1784) disposée entre les régions supérieure et inférieure afin qu'une surface de la région inférieure soit planaire,
un masque noir formé à une limite entre des électrodes adjacentes d'élément d'image (1787),
une couche (1773) de matière à cristaux liquides formée entre les premier et second substrats,
le premier substrat comprenant en outre un premier film isolant de couche (1778) qui recouvre les transistors à couches minces (1700),
un motif (1780) de lignes métalliques de bus connectées électriquement à une région de source (S) de chaque transistor à couches minces (1700) par un premier trou de contact (1779) formé dans le premier film isolant de couche (1778),
un second film isolant de couche (1781) recouvrant le motif de lignes métalliques de bus (1780) et le premier film isolant de couche (1778),
un film de passivation (1782) formé sur le second film isolant de couche (1781),
un masque noir comprenant un film d'ombrage (1783) formé sur le film de passivation au dessus d'une partie du transistor à couches minces (1700),
la couche de planarisation (1784) étant formée sur le film d'ombrage (1783) et le second film isolant de couche (1781),
l'électrode d'élément d'image (1787) étant connectée électriquement à une région de drain (D) du transistor à couches minces (1700) par un second trou (1785) passant dans la couche de planarisation (1784) et le second film isolant de couche (1781),
le masque noir comprenant en outre une couche d'ombrage (1786) qui recouvre l'intérieur et la périphérie du second trou de contact.

FIG. 1

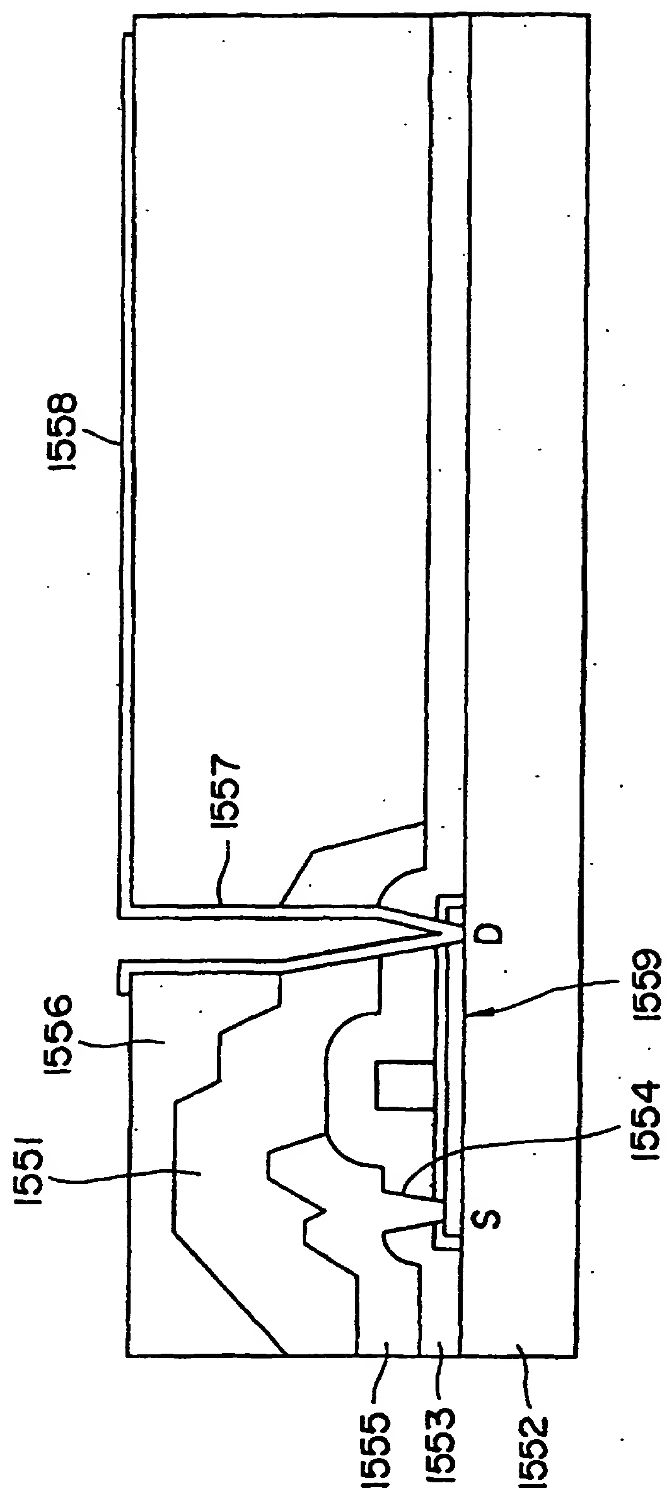

FIG. 2

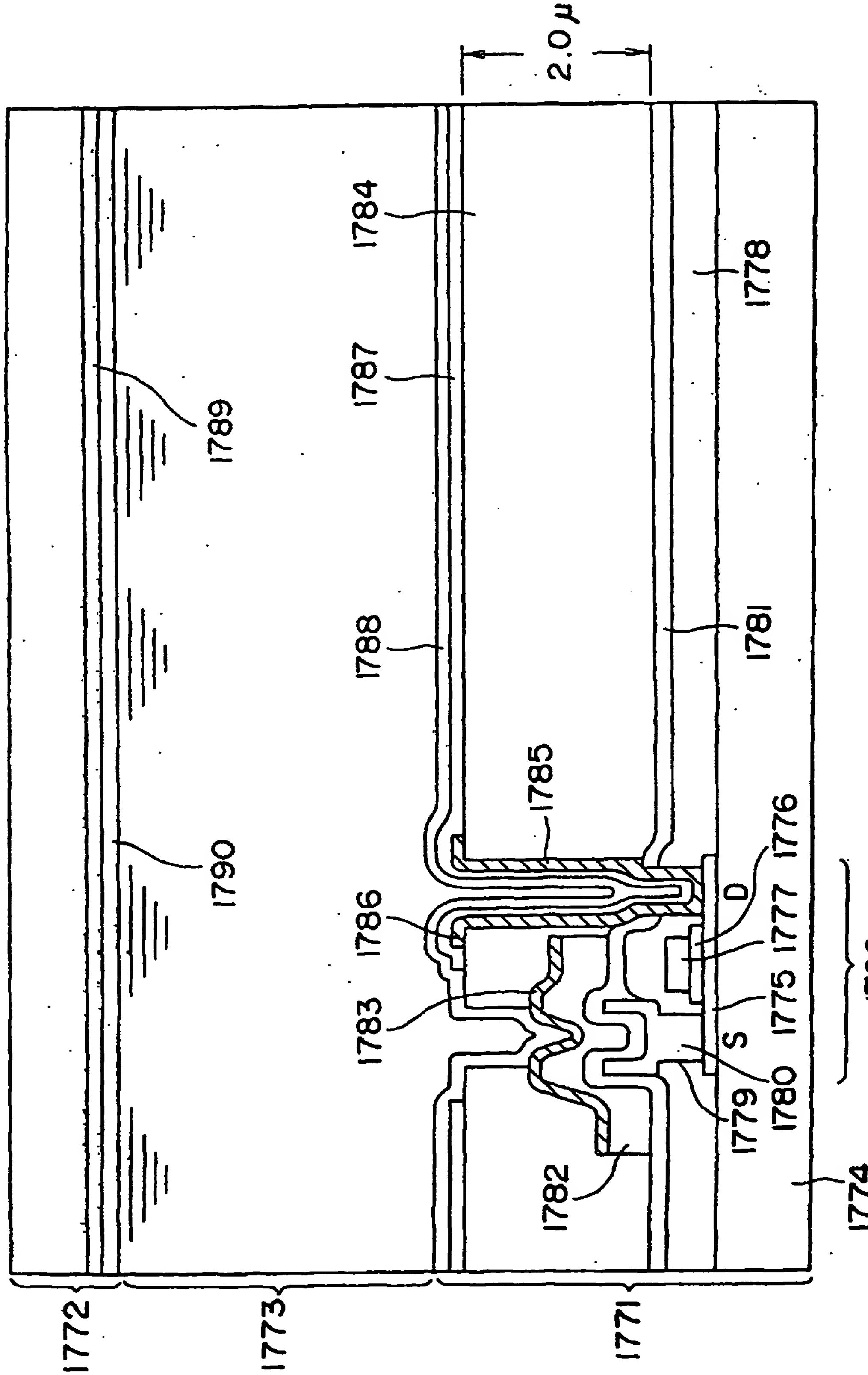
2.0μ
1784
1778
1787
1789
1788
1781
1785
1776
1790
1786
D
1777
1700
1775
1783
S
1780
1779
1782
1774
1772
1773
1771

FIG. 3
PRIOR ART

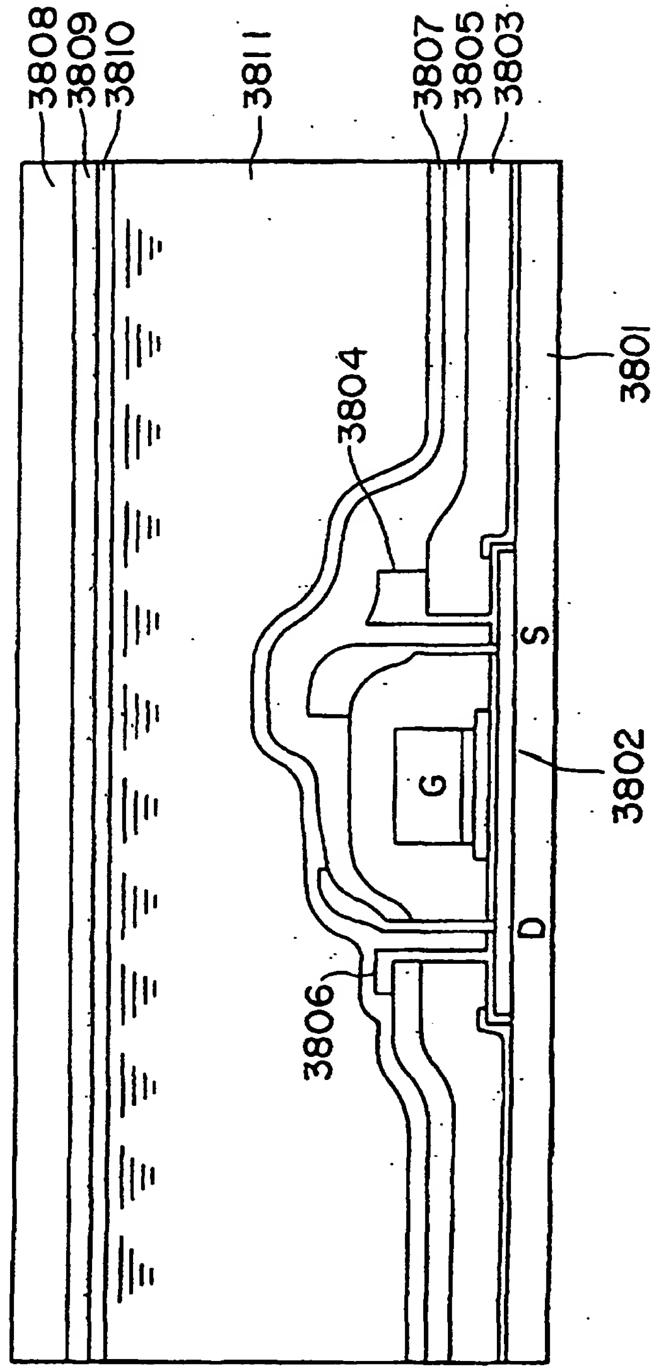

FIG. 4 PRIOR ART

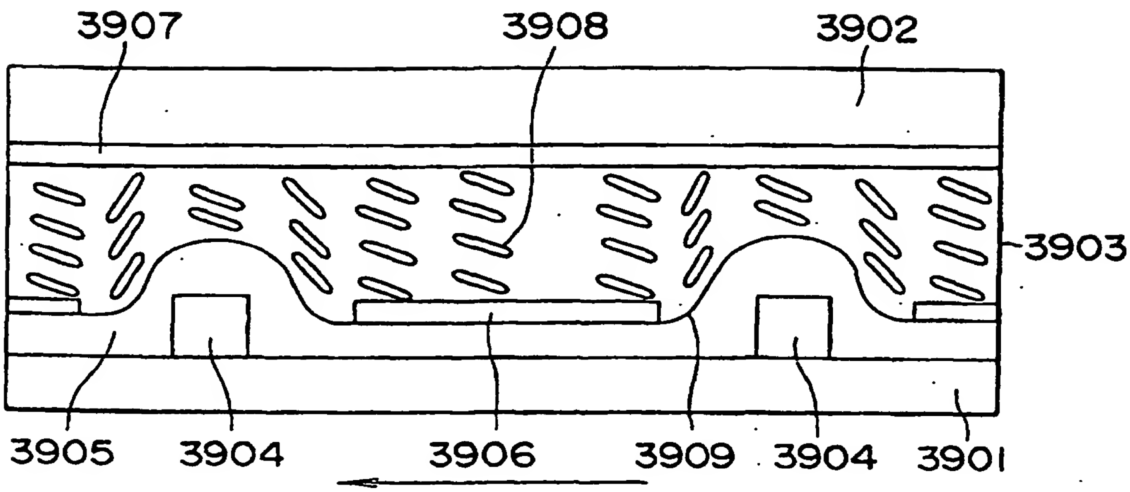

FIG. 5

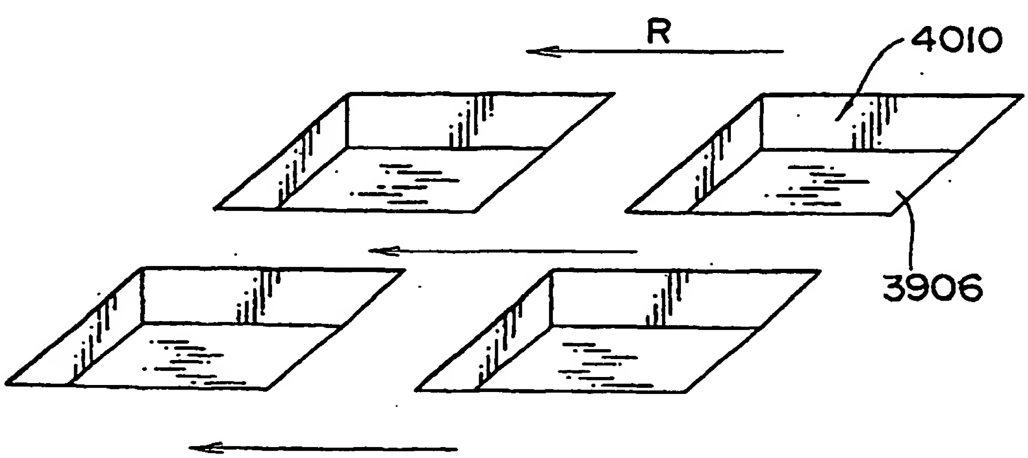

FIG. 6
PRIOR ART

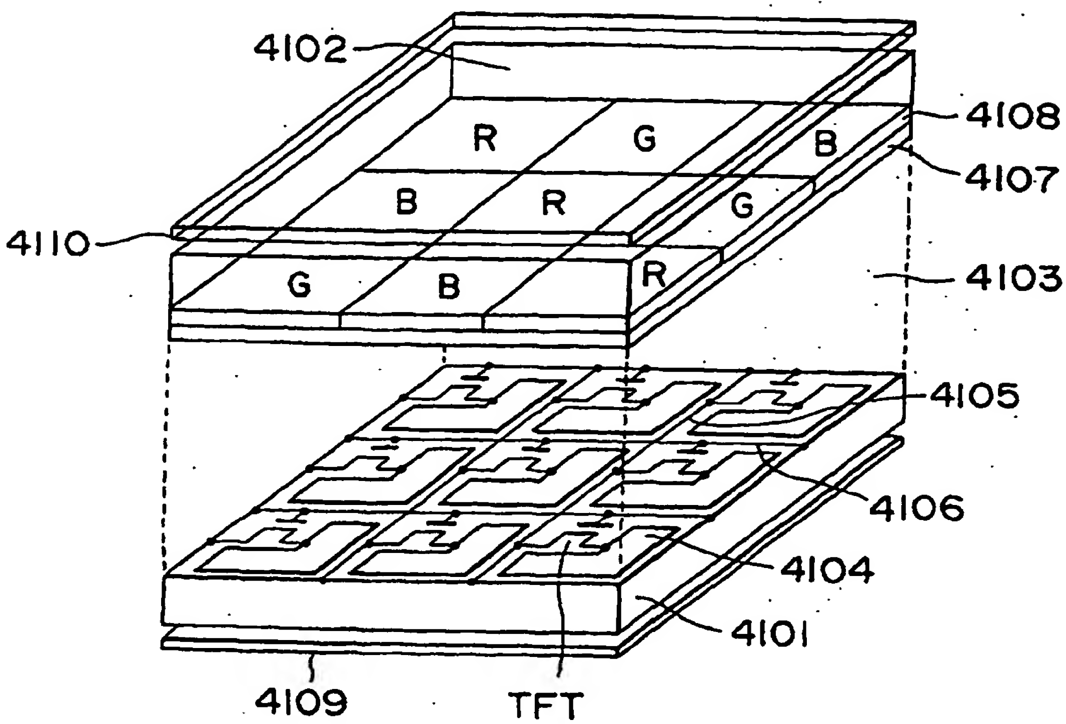

FIG. 7

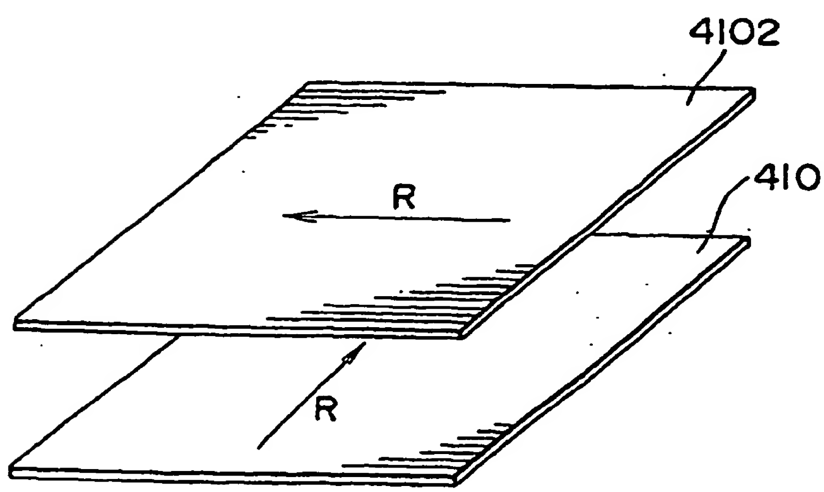

FIG. 8
PRIOR ART

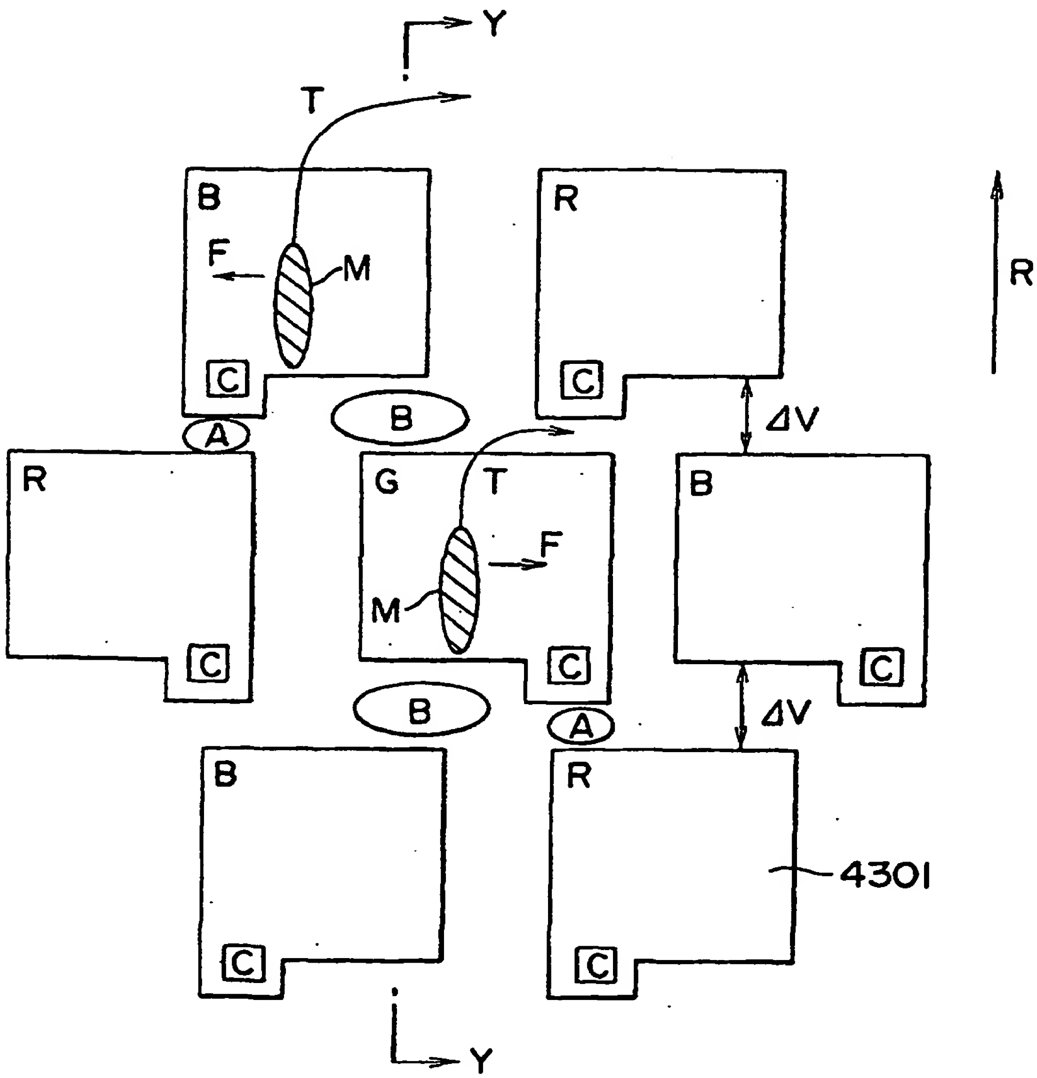

FIG. 9
PRIOR ART